Express Mail No. EV 346 810 419 US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Stephen Maxwell PARKES	Confirmation No. 4765
Application No.: 10/679,978	Group Art Unit: 2183
Filed: October 6, 2003	Examiner:
For: INTEGRATED CIRCUIT AND RELATED IMPROVEMENTS	Attorney Docket No.: 85170-4800

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Pursuant to applicant's duty of disclosure under 37 C.F.R. 1.56, enclosed are copies of fifteen (15) references for the Examiner's review and consideration. These references are listed on the enclosed Form PTO-1449.

It is respectfully requested that these references be made of record in this application by the Examiner's completion and return of the PTO Form 1449.

No fee is believed to be due for the filing of this statement as it is being submitted prior to an initial office action for this application. Should any fees be required, however, please charge such fees to Winston & Strawn Deposit Account No. 50-1814.

Respectfully submitted,

Date: 1/26/04

Allan A. Fanucci (Reg. No. 30,256)

WINSTON & STRAWN
CUSTOMER NO. 28765

(212) 294-3311

Enclosures

LIST OF REFERENCES CITED BY APPLICANT
(Use several sheets if necessary)

ATTY. DOCKET NO.:	APPLICATION SERIAL NO.:
85170-4800	10/679,978
APPLICANT: Stephen Maxwell Parkes	
FILING DATE: October 6, 2003	**GROUP:** 2183

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	4,569,041	2/1986	Takeuchi et al.	370	60	
	AB	6,072,944	6/2000	Robinson	395	500.05	
	AC						
	AD						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	AE	EP 0 338 558	10/1989	Europe			X	
	AF	EP 0 867 820	1/1998	Europe			X	
	AG	EP 0 969 631	1/2000	Europe			X	
	AH	EP 1 096 736	5/2001	Europe			X	
	AI	WO 98/02822	1/1998	PCT			x	

OTHER REFERENCES *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	AK	Parkes,"Space Wire: Links, Nodes, Routers and Networks" ECSS-E-50-12 Space Engineering pp. 1-101.
	AL	Swamy et al. "OO-VHDL, Extensions to VHDL" IEEE (1995)
	AM	Guerrier et al. "A Generic Architecture for On-Chip Packet-Switched Interconnections"
	AN	Benini et al. "Networks on Chips: A new SoC Paradigm" SOC Designs IEEE (2002)
	AO	A. Tsutsui et al., "Special Purpose FPGA for High-speed Digital Telecommuniation Systems", NTT Optical Network Systems Laboratories , pp 486-491, IEEE (1995)
	AP	D'Angelo et al., "Modular Design of Communication Node Prototypes" pp. 170-175 IEEE (1997)
	AQ	Kaptanoglu et al.,(XP-000868474) "A new high density and very low cost reprogrammable FPGA architecture"pp 3-12, (1999)
	AR	Vranesic "The FPGA Challenge", Dept. of Electrical and Compurter Engineering, pp 121-126 IEEE (1998).

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with **MPEP 609**; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.